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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
08/650,719	05/20/1996	JEFFREY S. MAILLOUX	95-0653	2941

21186 7590 05/07/2004

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EXAMINER	
KIM, HONG CHONG	
ART UNIT	**PAPER NUMBER**
2186	16

DATE MAILED: 05/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	08/650,719	MAILLOUX ET AL.	
	Examiner	Art Unit	
	Hong C Kim	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9,33-35,46,48-50,59-61,63 and 64* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,33-35,46,48-50,59-61,63 and 64* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *5/20/96* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

idl

Detailed Action

1. Claims 1-9, 33-35, 46, 48-50, 59-61, and 63-64 are presented for examination. This office action is in response to the Appeal Brief filed on 1/14/04.

2. Prosecution on the merits of this application is reopened on claims1-9, 33-35, 46, 48-50, 59-61, and 63-64, therefore, the finality of that action is withdrawn.

3. It is noted that this application appears to claim subject matter disclosed in the co-pending section or related section of this application. Applicants are reminded to maintain a clear line of demarcation between this application and co-pending or related applications to avoid possible double patenting (i.e. U.S Pat. No 5966724).

Drawings

4. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, a timing diagram of "while in the burst mode of operation, generating at least one subsequent internal address patterned after the initial external address provided while in the pipelined mode of operation" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

5. Claim 61 is objected to because of the following informalities: In line 5, it appears that "a burst" should be changed to – the pipelined—(see claim 46 lines 4-6, a new external address is provided in a pipelined mode) for consistency; in line 6, "the burst" should be changed to – a burst – for clarity; in line 8, that "pipelined" should be changed to – burst— (see claim 46 lines 8-9) for consistency. Appropriate correction is required.

DOUBLE-PATENTING

The non-statutory double patenting rejection, whether of the obviousness-type or non-obviousness-type, is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent. *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); and *In re Goodman*, 29 USPQ2d 2010 (Fed. Cir. 1993).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(b) and (c) may be used to overcome an actual or provisional rejection based on a non-statutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.78(d).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

6. Claim 61 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-23 of U.S. Patent No. 6,615,325. Claims 1-23 of patent 6,615,325 contain every element of claim 61 of the instant application and as such anticipates claim 61 of the instant application.
"A later patent claim is not patentably distinct from an earlier patent claim if the later claim is obvious over, or anticipated by, the earlier claim. In re Lonai, 759 F.2d at 896, 225 USPQ at 651 (affirming a holding of obviousness-type double patenting because the claims at issue were obvious over claims in four prior art patents); In re Berg, 140 F.3d at 1437, 46 USPQ2d at 1233 (Fed. Cir. 1998) (affirming a holding of obviousness-type double patenting where a patent application claim to a genus is anticipated by a patent claim to a species within that genus). " ELI LILLY AND COMPANY v BARR LABORATORIES, INC., United States Court of Appeals for the Federal Circuit, ON

PETITION FOR REHEARING EN BANC (DECIDED: May 30, 2001).

7. Claims 59-60 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 36 of copending Application No. 08/984,563. Although the conflicting claims are not identical, they are not patentably distinct from each other because both sets of claims are related to a method of accessing a storage device, comprising: a first address, burst and pipelined mode, selecting inputting and outputting information, selecting a burst mode and a pipelined mode, utilizing a second address to access data in a memory. Both sets of claims recited similar inventive concept of accessing a memory in burst and pipelined mode except: Claims 59-60 of the present invention comprises less specific steps than as claimed in the Application No. 08/984,563. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize teaching of 08/984,563 and modify an external row address to a first address and a first external column address to a second address of the copending application to arrive invention of the present application.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

8. Claim 61 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Because although the specification (pg.27, 1-11; pg.38, line 11-15; and pg. 39, lines 9-16) describes burst and pipeline operations as pointed out by the applicants in the brief, the specification does not specifically describe claimed limitation of "while in the burst mode of operation, generating at least one subsequent internal address patterned after the initial external address provided while in the pipelined mode of operation". On the contrary, application describes "switching between burst EDO and pipelined EDO modes is accomplished on successive /CAS cycles" (Pg 38 lines 11-15 and See Fig. 17 Refs 114 and 115, each /CAS cycle represents a new column address in pipeline mode). In other words, a new external address (Fig. 17 3rd addr) is needed after the initial external address (Fig. 17 2nd addr) to switch modes (also refer to claim 46 of the present application), however, applicant claimed generating at least one subsequent internal address patterned without a new external address. Therefore, "while in the burst mode of operation, generating at least one subsequent internal address patterned after the initial external address provided

while in the pipelined mode of operation" was not described in the specification

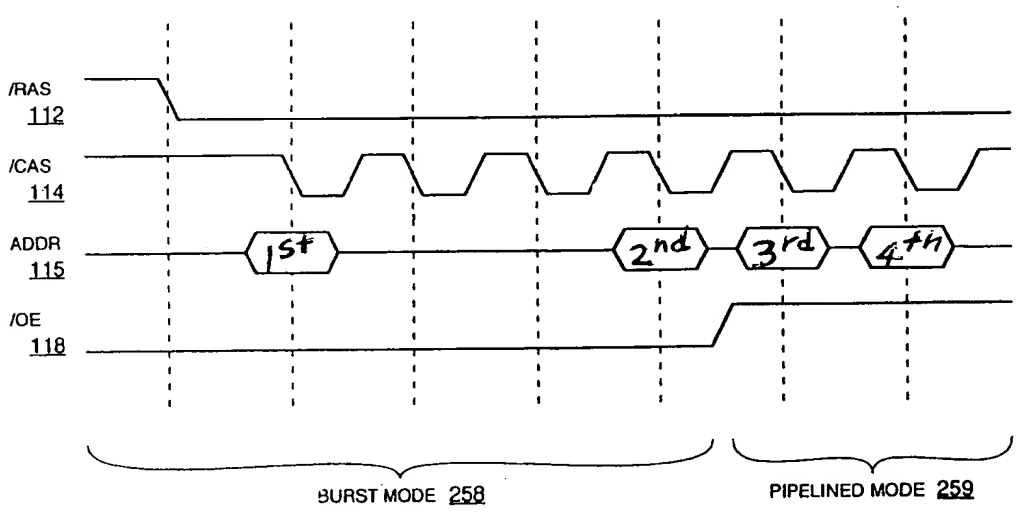

FIG. 17

Claim Rejections - 35 USC § 102/103

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-9, 33-35, 46, 48-50, 59-61, and 63-64 are rejected under 35 U.S.C. 102(e) as anticipated by *Manning*, U.S. Patent 5,610,864 or, in the alternative, under 35 U.S.C. 103(a) as obvious over by *Manning*, U.S. Patent 5,610,864 in view of Roy U.S. Patent No. 6,065,092.

As to claim 50, *Manning* discloses the invention as claimed. *Manning* discloses a system comprising: a microprocessor (Fig. 11 Ref. 112); a memory (Fig. 11 Ref. 124) coupled to the microprocessor, the memory selectively operable either in a burst mode (col. 6 lines 14-34 and col. 7 lines 43-54) or a pipelined mode (col. 5 lines 43-50, "Other memory architectures applicable to the current invention include a pipelined architecture

where memory access are performed sequentially" and col. 6 lines 14-16 "switching between burst EDO and standard EDO modes" read on this limitation, since standard EDO mode can include a pipeline architecture and it is inherent that the memory selectively operable in a pipelined mode because in order to work in a standard EDO memory including a pipeline architecture, one has to select a pipeline EDO mode), wherein the memory is an asynchronous dynamic random access memory (Fig. 1 and EDO constitutes asynchronous memory, col. col. 6 lines 14-16, since the EDO does not require a system clock to operate); and a system clock (col. 8 line 46) coupled to the microprocessor.

It is well known in the memory art that the pipelined memory architecture provides speed advantages by enabling more than one memory read, memory write, memory address input, memory data input or memory data output to be processed simultaneously. In other words, the pipeline architecture advantage in a memory effectively hides memory wait state; specifically this is accomplished by overlapping memory operations using a pipe. Another advantage that the pipelined memory architecture has over the parallel read and write architecture is a reduction in required circuitry. In particular, the parallel architecture requires two sample-and-hold circuits (one in each buffer) per read or write circuit. The pipelined architecture requires only a single sample-and-hold circuit per read or write circuit. Thus, the pipelined architecture can reduce circuit cost by decreasing the required integrated circuit area.

Even if the system does not include the memory selectively operable in a pipelined mode. It was well known in the memory art to include the memory selectively operable in a pipelined mode in the same field of endeavor for the purpose of increasing the throughput by accessing the memory every cycle.

Roy discloses the memory selectively operable in a pipelined mode (col. 27 line 35 thru col. 28 line 48 specifically col. 28 lines 16- 48 and col. 21 lines 61-62) for the purpose of providing a new column address every cycle (col. 28 lines 19-25) thereby increasing the throughput by one-half the normal access frequency (col. 28 lines 29-32).

One of ordinary skill in the memory art familiar with Manning, and looking at Roy would have recognized that the memory access performance of Manning would have been enhanced by including a pipelined mode in the memory because it would provide a new column address every cycle thereby increasing the memory throughput or speed. The ability to provide a new column address every cycle would have a highly desirable feature in the memory environment of Manning because one of the objective of memory access is increasing throughput or speed. Also the ability to increase the throughput by accessing the memory every cycle provides sufficient suggestion and motivation to one of ordinary skill in the memory art to include the memory selectively operable in a pipelined mode.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to include the memory selectively operable in a pipelined mode of Roy in the invention of Manning because it would increase memory

performance of Manning by providing a new column address every cycle thereby increasing the memory throughput or speed in Manning.

As to claim 63, *Manning* discloses a storage device, comprising; an array of memory cells (col. 4 lines 13-15); mode circuitry for receiving a burst/pipeline signal (col. 5 lines 41-50, col. 6 lines 14-34 & col. 7 lines 43-54 "Other memory architectures applicable to the current invention include a pipelined architecture where memory access are performed sequentially" and col. 6 lines 14-16 "switching between burst EDO and standard EDO modes" read on this limitation, since standard EDO mode can include a pipeline architecture and also it is inherent that the memory include mode circuitry for receiving a pipeline signal because in order to work in a standard EDO memory including a pipeline architecture, one has to select a pipeline EDO mode); and operation circuitry operable in a burst or a pipeline mode of operation depending upon the burst/pipeline signal, the operation circuitry switchable between burst and pipeline modes of operation (col. 5 lines 41-50, col. 6 lines 14-34, and col. 7 lines 43-54). Also it is well known in the memory art that the pipelined memory architecture provides speed advantages by enabling more than one memory read, memory write, memory address input, memory data input or memory data output to be processed simultaneously. In other words, the pipeline architecture advantage in a memory effectively hides memory wait state; specifically this is accomplished by overlapping memory operations using a pipe. Another advantage that the pipelined memory architecture has over the parallel

read and write architecture is a reduction in required circuitry. In particular, the parallel architecture requires two sample-and-hold circuits (one in each buffer) per read or write circuit. The pipelined architecture requires only a single sample-and-hold circuit per read or write circuit. Thus, the pipelined architecture can reduce circuit cost by decreasing the required integrated circuit area.

Even if the system does not include mode circuitry for receiving a pipeline signal. It was well known in the memory art to include mode circuitry for receiving a pipeline signal in the memory in the same field of endeavor for the purpose of increasing the throughput by accessing the memory every cycle.

Roy discloses mode circuitry for receiving a pipeline signal (col. 27 line 35 thru col. 28 line 48 specifically col. 28 lines 16- 48 and col. 21 lines 61-62) for the purpose of providing a new column address every cycle (col. 28 lines 19-25) thereby increasing the throughput by one-half the normal access frequency (col. 28 lines 29-32).

One of ordinary skill in the memory art familiar with Manning, and looking at Roy would have recognized that the memory access performance of Manning would have been enhanced by including a pipelined mode in the memory because it would provide a new column address every cycle thereby increasing the memory throughput or speed. The ability to provide a new column address every cycle would have a highly desirable feature in the memory environment of Manning because one of the objective of memory access is increasing throughput or speed. The ability to increase the throughput by accessing the memory every cycle provides sufficient suggestion and motivation to one

of ordinary skill in the memory art to include mode circuitry for receiving a pipeline signal in the memory.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to include mode circuitry for receiving a pipeline signal the memory of Roy in the invention of Manning because it would increase memory performance of Manning by providing a new column address every cycle thereby increasing the memory throughput or speed in Manning.

As to claim 1, *Manning* discloses the invention as claimed. *Manning* discloses an asynchronously accessible storage device (Fig. 1 and EDO constitutes asynchronous memory, col. col. 6 lines 14-16, since the EDO does not require a system clock to operate) comprising mode circuitry to select between a burst mode (col. 6 lines 14-34 and col. 7 lines 43-54) and a pipelined mode (col. 5 lines 43-50, "Other memory architectures applicable to the current invention include a pipelined architecture where memory access are performed sequentially" and col. 6 lines 14-16 "switching between burst EDO and standard EDO modes" read on this limitation, since standard EDO mode can include a pipeline architecture and also it is inherent that the memory include mode circuitry to select a pipeline mode because in order to work in a standard EDO memory including a pipeline architecture, one has to select a pipeline EDO mode); and circuitry operable in either the burst mode or the pipelined mode coupled to the mode selection circuitry and configure to select between two modes.(Fig. 1 Ref. 40 and col. 6 lines 14-

16 & col. 5 lines 41-50). Also it is well known in the memory art that the pipelined memory architecture provides speed advantages by enabling more than one memory read, memory write, memory address input, memory data input or memory data output to be processed simultaneously. In other words, the pipeline architecture advantage in a memory effectively hides memory wait state; specifically this is accomplished by overlapping memory operations using a pipe. Another advantage that the pipelined memory architecture has over the parallel read and write architecture is a reduction in required circuitry. In particular, the parallel architecture requires two sample-and-hold circuits (one in each buffer) per read or write circuit. The pipelined architecture requires only a single sample-and-hold circuit per read or write circuit. Thus, the pipelined architecture can reduce circuit cost by decreasing the required integrated circuit area.

Even if the system does not include mode circuitry to select a pipeline mode. It was well known in the memory art to include mode circuitry to select a pipeline mode in the memory in the same field of endeavor for the purpose of increasing the throughput by accessing the memory every cycle.

Roy discloses mode circuitry to select a pipeline mode (col. 27 line 35 thru col. 28 line 48 specifically col. 28 lines 16- 48 and col. 21 lines 61-62) for the purpose of providing a new column address every cycle (col. 28 lines 19-25) thereby increasing the throughput by one-half the normal access frequency (col. 28 lines 29-32).

One of ordinary skill in the memory art familiar with Manning, and looking at Roy would have recognized that the memory access performance of Manning would have

been enhanced by including a pipelined mode in the memory because it would provide a new column address every cycle thereby increasing the memory throughput or speed. The ability to provide a new column address every cycle would have a highly desirable feature in the memory environment of Manning because one of the objective of memory access is increasing throughput or speed. Also the ability to increase the throughput by accessing the memory every cycle provides sufficient suggestion and motivation to one of ordinary skill in the memory art to include mode circuitry to select a pipeline mode.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to include mode circuitry to select a pipeline mode of Roy in the invention of Manning because it would increase memory performance of Manning by providing a new column address every cycle thereby increasing the memory throughput or speed in Manning.

As to claim 2, Manning further discloses the burst mode and the pipelined mode are EDO modes of operation (col. 5 lines 41-50, col. 6 lines 14-34 and col. 7 lines 43-54)

As to claim 3, Manning further discloses the pipelined mode is an EDO mode (col. 5 lines 41-50, col. 6 lines 14-34 and col. 7 lines 43-54).

As to claim 4, Manning further discloses the burst mode is and EDO mode (col. 6 line 15).

As to claim 5, Manning further discloses the mode circuitry includes a buffer, the buffer for storing an address (Fig. 1 Refs. 18, 22, and 30).

As to claim 6, Manning further discloses the mode circuitry includes at least one counter for incrementing the address (Fig. 1 Ref. 26 and col.5 lines 51-62).

As to claim 7, Manning further discloses the mode circuitry includes receiving an external address (Fig. 1 Ref. 16 and col. 4 lines 16-28).

As to claim 8, Manning further discloses the mode circuitry includes a buffer, the buffer for storing an address (Fig. 1 Refs. 18, 22, and 30).

As to claim 9, Manning further discloses the mode circuitry includes multiplexed device for providing an internally generated address to the storage device (Fig. 1 Refs. 26 and 30 and col. 5 lines 51-62 & col. 3 lines 20-23, selection of external or internal address reads on this limitation).

As to claims 33, 59, and 60, *Manning* discloses a method for accessing a storage device (Fig. 1), comprising: receiving a first address to the storage device (Fig. 2 ROW); selecting between an asynchronously accessible (Fig. 1 and EDO constitutes asynchronous operation, col. col. 6 lines 14-16) burst mode (col. 6 lines 14-26 and col. 7 lines 43-54) and a pipelined mode (col. 5 lines 43-50, "Other memory architectures applicable to the current invention include a pipelined architecture where memory access are performed sequentially" and col. 6 lines 14-16 "switching between burst EDO and standard EDO mode" read on this limitation, since standard EDO mode can include a pipeline architecture also it is inherent that the memory include a pipeline mode because in order to work in a standard EDO memory including a pipeline architecture, one has to select a pipeline EDO mode) of operations of the storage device; selecting between outputting information from the storage device and inputting to the storage device (Fig. 2 /WE, read and write operations read on this limitation); obtaining a second address to the storage device (Fig. 2 /COL), and asynchronously accessing a storage element of the storage device in the selected mode of operation using the first address and the second addresses (Fig. 2, DQ and col. 5 lines 41-50, col. 6 lines 14-26 & col. 7 lines 43-54). Also it is well known in the memory art that the pipelined memory architecture provides speed advantages by enabling more than one memory read, memory write, memory address input, memory data input or memory data output to be processed simultaneously. In other words, the pipeline architecture advantage in a memory effectively hides memory wait state; specifically this is

accomplished by overlapping memory operations using a pipe. Another advantage that the pipelined memory architecture has over the parallel read and write architecture is a reduction in required circuitry. In particular, the parallel architecture requires two sample-and-hold circuits (one in each buffer) per read or write circuit. The pipelined architecture requires only a single sample-and-hold circuit per read or write circuit. Thus, the pipelined architecture can reduce circuit cost by decreasing the required integrated circuit area.

Even if the system does not include a pipeline mode. It was well known in the memory art to include a pipeline mode in the memory in the same field of endeavor for the purpose of increasing the throughput by accessing the memory every cycle.

Roy discloses a pipeline mode (col. 27 line 35 thru col. 28 line 48 specifically col. 28 lines 16- 48 and col. 21 lines 61-62) for the purpose of providing a new column address every cycle (col. 28 lines 19-25) thereby increasing the throughput by one-half the normal access frequency (col. 28 lines 29-32).

One of ordinary skill in the memory art familiar with Manning, and looking at Roy would have recognized that the memory access performance of Manning would have been enhanced by including a pipelined mode in the memory because it would provide a new column address every cycle thereby increasing the memory throughput or speed. The ability to provide a new column address every cycle would have a highly desirable feature in the memory environment of Manning because one of the objective of memory access is increasing throughput or speed. Also the ability to increase the throughput by

accessing the memory every cycle provides sufficient suggestion and motivation to one of ordinary skill in the memory art to include a pipeline mode.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to include a pipeline mode of Roy in the invention of Manning because it would increase memory performance of Manning by providing a new column address every cycle thereby increasing the memory throughput or speed in Manning.

As to claim 34, Manning further discloses a step of switching between the pipelined mode and burst mode (col. 5 lines 41-50, col. 6 lines 14-16 and col. 5 lines 42-50).

Roy also further discloses a step of switching between the pipelined mode and burst mode (col. 27 lines 35 thru col. 28 lines 48 and col. 21 lines 61-62 specifically col. 27 lines 54-58)

As to claim 35, Manning further discloses the second address is an external address (Fig. 1 Refs 16 and 30 and col. 4 lines 16-28 & col. 5 lines 42-55). Roy also further discloses the second address is an external address (col. 28 lines 16-25).

As to claim 46, *Manning* discloses a method for accessing several different locations in an asynchronously a storage device (Fig. 1 and EDO constitutes

asynchronous operation, col. col. 6 lines 14-16), comprising: selecting a pipelined mode of operation (col. 5 lines 43-50, "Other memory architectures applicable to the current invention include a pipelined architecture where memory access are performed sequentially" and col. 6 lines 14-16 "switching between burst EDO and standard EDO mode" read on this limitation, since standard EDO mode can include a pipeline architecture also it is inherent that the memory include a pipeline mode because in order to work in a standard EDO memory including a pipeline architecture, one has to select a pipeline EDO mode); providing a new external addresses for every access associated with accessing the asynchronously-accessible memory device while in the pipelined mode of operation (col. 5 lines 42-50, "where memory accesses are performed sequentially" and "one access per cycle" read on this limitation); switching a burst mode of operation (col. 6 lines 14-26 and col. 7 lines 43-54); providing an initial external address associated with asynchronously accessing the asynchronously-accessible memory device in the burst mode of operation (col. 5 lines 51-62 and col. 8 line 67); and generating at least one subsequent internal address patterned after the initial external address while in the burst mode of operation (col. 5 lines 51-62 and col. 8 line 67). Also it is well known in the memory art that the pipelined memory architecture provides speed advantages by enabling more than one memory read, memory write, memory address input, memory data input or memory data output to be processed simultaneously. In other words, the pipeline architecture advantage in a memory effectively hides memory wait state; specifically this is accomplished by overlapping

memory operations using a pipe. Another advantage that the pipelined memory architecture has over the parallel read and write architecture is a reduction in required circuitry. In particular, the parallel architecture requires two sample-and-hold circuits (one in each buffer) per read or write circuit. The pipelined architecture requires only a single sample-and-hold circuit per read or write circuit. Thus, the pipelined architecture can reduce circuit cost by decreasing the required integrated circuit area.

Even if the system does not include a pipeline mode and provide a new external address for every access. It was well known in the memory art to include a pipeline mode in the memory and provide a new external address for every access in the same field of endeavor for the purpose of increasing the throughput by accessing the memory every cycle.

Roy discloses a pipeline mode and a new external address for every access (col. 27 line 35 thru col. 28 line 48 specifically col. 28 lines 16- 48 and col. 21 lines 61-62) for the purpose of providing a new column address every cycle (col. 28 lines 19-25) thereby increasing the throughput by one-half the normal access frequency (col. 28 lines 29-32).

One of ordinary skill in the memory art familiar with Manning, and looking at Roy would have recognized that the memory access performance of Manning would have been enhanced by including a pipelined mode in the memory because it would provide a new column address every cycle thereby increasing the memory throughput or speed. The ability to provide a new column address every cycle would have a highly desirable feature in the memory environment of Manning because one of the objective of memory

access is increasing throughput or speed. Also the ability to increase the throughput by accessing the memory every cycle provides sufficient suggestion and motivation to one of ordinary skill in the memory art to include a pipeline mode.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to include a pipeline mode and providing a new external address for every access of Roy in the invention of Manning because it would increase memory performance of Manning by providing a new column address every cycle thereby increasing the memory throughput or speed in Manning.

As to claims 48 and 49, Roy further discloses column, row, application, fixed access based switching (col. 27 lines 54-58) for the burst mode and the pipelined mode.

As to claim 61, *Manning* discloses a method for accessing several different locations in an asynchronously a storage device (Fig. 1 and EDO constitutes asynchronous operation, col. col. 6 lines 14-16), comprising: selecting a pipelined mode of operation (col. 5 lines 43-50, "Other memory architectures applicable to the current invention include a pipelined architecture where memory access are performed sequentially" and col. 6 lines 14-16 "switching between burst EDO and standard EDO modes" read on this limitation, since standard EDO mode can include a pipeline architecture also it is inherent that the memory include a pipeline mode because in order to work in a standard EDO memory including a pipeline architecture, one has to

select a pipeline EDO mode); providing a new external addresses for every access associated with accessing the asynchronously-accessible memory device while in the pipelined mode of operation (col. 5 lines 42-50, definition of the pipeline "where memory accesses are performed sequentially" and "one access per cycle" reads on this limitation); switching a burst mode of operation (col. 6 lines 14-34 and col. 7 lines 43-54); providing an initial external address associated with asynchronously accessing the asynchronously-accessible memory device in the burst mode of operation (col. 5 lines 51-62 and col. 8 line 67); and generating at least one subsequent internal address patterned after the initial external address while in the burst mode of operation (col. 5 lines 51-62 and col. 8 line 67). Also it is well known in the memory art that the pipelined memory architecture provides speed advantages by enabling more than one memory read, memory write, memory address input, memory data input or memory data output to be processed simultaneously. In other words, the pipeline architecture advantage in a memory effectively hides memory wait state; specifically this is accomplished by overlapping memory operations using a pipe. Another advantage that the pipelined memory architecture has over the parallel read and write architecture is a reduction in required circuitry. In particular, the parallel architecture requires two sample-and-hold circuits (one in each buffer) per read or write circuit. The pipelined architecture requires only a single sample-and-hold circuit per read or write circuit. Thus, the pipelined architecture can reduce circuit cost by decreasing the required integrated circuit area.

Even if the system does not include a pipeline mode and provide a new external address for every access. It was well known in the memory art to include a pipeline mode in the memory and provide a new external address for every access in the same field of endeavor for the purpose of increasing the throughput by accessing the memory every cycle.

Roy discloses a pipeline mode and a new external address for every access (col. 27 line 35 thru col. 28 line 48 specifically col. 28 lines 16- 48 and col. 21 lines 61-62) for the purpose of providing a new column address every cycle (col. 28 lines 19-25) thereby increasing the throughput by one-half the normal access frequency (col. 28 lines 29-32).

One of ordinary skill in the memory art familiar with Manning, and looking at Roy would have recognized that the memory access performance of Manning would have been enhanced by including a pipelined mode in the memory because it would provide a new column address every cycle thereby increasing the memory throughput or speed. The ability to provide a new column address every cycle would have a highly desirable feature in the memory environment of Manning because one of the objective of memory access is increasing throughput or speed. Also the ability to increase the throughput by accessing the memory every cycle provides sufficient suggestion and motivation to one of ordinary skill in the memory art to include a pipeline mode.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to include a pipeline mode and providing a new external address for every access of Roy in the invention of Manning because it would

increase memory performance of Manning by providing a new column address every cycle thereby increasing the memory throughput or speed in Manning.

As to claim 64, *Manning* discloses a memory circuit, comprising; an array of memory cells (col. 4 lines 13-15); burst/pipeline selection circuitry for determining a burst or a pipeline mode of operation of the memory circuit (col. 5 lines 41-50, col. 6 lines 14-34 & col. 7 lines 43-54, "Other memory architectures applicable to the current invention include a pipelined architecture where memory access are performed sequentially" and col. 6 lines 14-16 "switching between burst EDO and standard EDO modes" read on this limitation, since standard EDO mode can include a pipeline architecture also it is inherent that the memory include a pipeline mode because in order to work in a standard EDO memory including a pipeline architecture, one has to select a pipeline EDO mode); and mode circuitry capable of operation in either a burst mode or a pipeline mode of operation, and switchable between burst and pipeline modes of operation (col. 5 lines 41-50, col. 6 lines 14-34, and col. 7 lines 43-54). Also it is well known in the memory art that the pipelined memory architecture provides speed advantages by enabling more than one memory read, memory write, memory address input, memory data input or memory data output to be processed simultaneously. In other words, the pipeline architecture advantage in a memory effectively hides memory wait state; specifically this is accomplished by overlapping memory operations using a pipe. Another advantage that the pipelined memory

architecture has over the parallel read and write architecture is a reduction in required circuitry. In particular, the parallel architecture requires two sample-and-hold circuits (one in each buffer) per read or write circuit. The pipelined architecture requires only a single sample-and-hold circuit per read or write circuit. Thus, the pipelined architecture can reduce circuit cost by decreasing the required integrated circuit area.

Even if the system does not include a pipelined mode circuitry. It was well known in the memory art to include in a pipelined mode in the same field of endeavor for the purpose of increasing the throughput by accessing the memory every cycle.

Roy discloses a pipelined mode (col. 27 line 35 thru col. 28 line 48 specifically col. 28 lines 16- 48 and col. 21 lines 61-62) for the purpose of providing a new column address every cycle (col. 28 lines 19-25) thereby increasing the throughput by one-half the normal access frequency (col. 28 lines 29-32).

One of ordinary skill in the memory art familiar with Manning, and looking at Roy would have recognized that the memory access performance of Manning would have been enhanced by including a pipelined mode in the memory because it would provide a new column address every cycle thereby increasing the memory throughput or speed. The ability to provide a new column address every cycle would have a highly desirable feature in the memory environment of Manning because one of the objective of memory access is increasing throughput or speed. The ability to increase the throughput by accessing the memory every cycle provides sufficient suggestion and motivation to one

of ordinary skill in the memory art to include the memory selectively operable in a pipelined mode.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to include a pipelined mode circuitry of Roy in the invention of Manning because it would increase memory performance of Manning by providing a new column address every cycle thereby increasing the memory throughput or speed in Manning.

Response to Amendment

9. Applicant's arguments filed on 1/16/04 have been fully considered but they are not persuasive.

A. In response to applicant's argument at the top of page 4 in the Appeal Brief that claim 61 is described in the Application as filed at the time the application was filed has been fully considered but it is not persuasive.

Claim 61 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Because although the specification (pg.27, 1-11; pg.38, line 11-15; and pg. 39, lines 9-16) describes burst and pipeline operations as pointed out by the applicants in the brief, the specification does not specifically describe claimed limitation of "while in the burst

mode of operation, generating at least one subsequent internal address patterned after the initial external address provided while in the pipelined mode of operation". It appear that pages 27, 36, and 38 only describes individual burst mode operation and pipelined operation. On the contrary, application describes "switching between burst EDO and pipelined EDO modes is accomplished on successive /CAS cycles" (Pg 38 lines 11-15 and See Fig. 17 Refs 114 and 115, each /CAS cycle represents a new column address in pipeline mode). In other words, a new external address (Fig. 17 3rd addr) is needed after the initial external address (Fig. 17 2nd addr) to switch modes (also refer to claim 46 of the present application), however, applicant claimed generating at least one subsequent internal address patterned without a new external address. Therefore, "while in the burst mode of operation, generating at least one subsequent internal address patterned after the initial external address provided while in the pipelined mode of operation" was not described in the specification. Again applicants are requested to point out this limitation of "while in the burst mode of operation, generating at least one subsequent internal address patterned after the initial external address provided while in the pipelined mode of operation" **in the drawing and in the specification**.

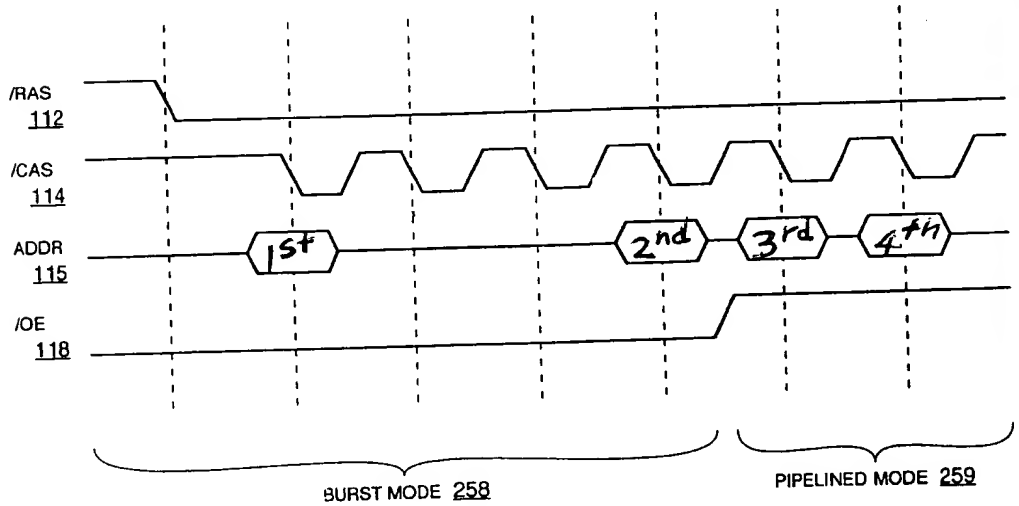
/RAS
112
/CAS
114
ADDR
115
/OE
118
1st
2nd
3rd
4th
BURST MODE 258
PIPELINED MODE 259

FIG. 17

B. In response to applicant's argument on page 6 in the Appeal Brief that the cited reference does not disclose switching between a burst mode and a pipelined mode of operation has been fully considered but it is not persuasive.

Manning (864) discloses the limitation of switching between a burst mode and a pipelined mode of operation, "The current invention include a pipelined architecture where memory accesses are performed sequentially" (col. 5 lines 43-49 in Manning) and "switching between burst EDO mode and standard EDO mode" (see col. 6 lines 14-16 & Fig. 1 and col. 7 lines 44-55 in Manning) read on this limitation. In other words, pipeline architecture can be applicable to a standard EDO memory and an external addresses are provided sequentially to the standard EDO memory. Also, this feature is inherent because in order to work in order to work in the current invention (i.e. a standard EDO memory) including a pipelined architecture, one has to select a pipelined mode if one was in a burst mode. Also it is well known in the memory art that the pipelined memory architecture provides speed advantages by enabling more than one memory read, memory write, memory address input, memory data input or memory data output to be processed simultaneously. In other words, the pipelined architecture advantage in a memory effectively hides memory wait state; specifically this is accomplished by overlapping memory operations using a pipe. Another advantage that the pipelined memory architecture has over the parallel read and write architecture is a reduction in required circuitry. In particular, the parallel architecture requires two sample-and-hold circuits (one in each buffer) per read or write circuit. The pipelined

architecture requires only a single sample-and-hold circuit per read or write circuit. Thus, the pipelined architecture can reduce circuit cost by decreasing the required integrated circuit area.

Even if the system does not include a pipelined mode circuitry. It was well known in the memory art to include in a pipelined mode in the same field of endeavor for the purpose of increasing the throughput by accessing the memory every cycle.

Roy discloses a pipelined mode (col. 27 line 35 thru col. 28 line 48 specifically col. 28 lines 16- 48 and col. 21 lines 61-62) for the purpose of providing a new column address every cycle (col. 28 lines 19-25) thereby increasing the throughput by one-half the normal access frequency (col. 28 lines 29-32).

One of ordinary skill in the memory art familiar with Manning, and looking at Roy would have recognized that the memory access performance of Manning would have been enhanced by including a pipelined mode in the memory because it would provide a new column address every cycle thereby increasing the memory throughput or speed. The ability to provide a new column address every cycle would have a highly desirable feature in the memory environment of Manning because one of the objective of memory access is increasing throughput or speed. The ability to increase the throughput by accessing the memory every cycle provides sufficient suggestion and motivation to one of ordinary skill in the memory art to include the memory selectively operable in a pipelined mode.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to include a pipelined mode circuitry of Roy in the invention of Manning because it would increase memory performance of Manning by providing a new column address every cycle thereby increasing the memory throughput or speed in Manning.

Therefore, prior arts disclose the limitation of switching between a burst mode and a pipelined mode of operation.

C. In response to applicant's argument at the top of page 8 in the Appeal Brief that the present application is allowable since application 08/984,561 is allowed has been fully considered but it is not persuasive.

The Examiner allowed application 08/984,561, now U.S. Patent No. 6,615,325, because it claimed mode circuitry to switch between the pipelined mode and burst mode of operation while maintaining a RAS in an active state and cycling a CAS to access data in the pipelined/burst mode and together with combination of other claimed element as set forth in the claims. In other words, application 08/984,561 claimed different claim limitations than the present application (see comparison chart below for claim1 of the present application and claim 20 of Patent No. 6,615,325 (08/984,561)).

08/650,719	Patent No. 6615325 (08/984,561)
1. An asynchronously accessible storage device comprising: **mode circuitry to select between a burst mode and a pipelined mode; and**	**20. A method for switching between pipeline and burst modes of operation, comprising:** **maintaining a first enabling signal in an active state, the first enabling signal being an address-**

circuitry operable in either the burst mode or the pipelined mode coupled to the mode selection circuitry and configure to switch between the pipelined mode and the burst mode for operating the asynchronously-accessible storage device in either mode.	**strobe signal;** **maintaining an external mode select signal to select a pipeline mode;** **receiving a stream of addresses and cycling a second enabling signal for processing the stream of addresses; and** **switching the mode of operation to a burst mode on successive cycles of the second enabling signal while maintaining the first enabling signal in the active state.**

D. In response to applicant's argument at the top of page 9 thru page 10 in the Appeal Brief that the cited reference does not disclose pipeline mode has been fully considered but it is not persuasive.

" Other memory architectures applicable to the current invention include a pipelined architecture where memory accesses are performed sequentially" (col. 5 lines 43-49 in Manning) read on this limitation since standard EDO mode can include a pipeline architecture also it is inherent that the memory include a pipeline mode because in order to work in a standard EDO memory including a pipeline architecture, one has to select a pipeline EDO mode. Also it is well known in the memory art that the pipelined memory architecture provides speed advantages by enabling more than one memory read, memory write, memory address input, memory data input or memory data output to be processed simultaneously. In other words, the pipelined architecture advantage in a memory effectively hides memory wait state; specifically this is accomplished by overlapping memory operations using a pipe. Another advantage that the pipelined memory architecture has over the parallel read and write architecture is a reduction in required circuitry. (See, for example, a pipeline operation is disclosed by Swoboda et al. (U.S. Patent No. 5,564,028) in Figs. 1-3 and col. 3 lines 15+. In Fig. 3, each address is provided to a memory every cycle in a pipeline fashion to fetch data from the memory. U.S. Patent No. 5,564,028 is included as Appendix I.) Therefore, Manning (864) discloses a pipelined mode (col. 5 lines 43-49).

Even if the system does not include a pipeline mode and provide a new external address for every access. It was well known in the memory art to include a pipeline mode in the memory and provide a new external address for every access in the same field of endeavor for the purpose of increasing the throughput by accessing the memory every cycle.

Roy discloses a pipeline mode and a new external address for every access (col. 27 line 35 thru col. 28 line 48 specifically col. 28 lines 16- 48 and col. 21 lines 61-62) for the purpose of providing a new column address every cycle (col. 28 lines 19-25) thereby increasing the throughput by one-half the normal access frequency (col. 28 lines 29-32).

One of ordinary skill in the memory art familiar with Manning, and looking at Roy would have recognized that the memory access performance of Manning would have been enhanced by including a pipelined mode in the memory because it would provide a new column address every cycle thereby increasing the memory throughput or speed. The ability to provide a new column address every cycle would have a highly desirable feature in the memory environment of Manning because one of the objective of memory access is increasing throughput or speed. Also the ability to increase the throughput by accessing the memory every cycle provides sufficient suggestion and motivation to one of ordinary skill in the memory art to include a pipeline mode.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to include a pipeline mode and providing a new external address for every access of Roy in the invention of Manning because it would

increase memory performance of Manning by providing a new column address every cycle thereby increasing the memory throughput or speed in Manning.

E. In response to applicant's argument at the top of page 14 in the Appeal Brief that applicant submit a Terminal Disclaimer to obviate any remaining double patenting rejections upon receiving an indication of allowance for claim in the instant application has been fully considered but it is not persuasive.

The Examiner maintains the double patenting rejection set forth in prior Office Action, Paper No. 42 (mailed out 5/12/2003), because the Appeal Brief does not specifically point out the supposed errors in the examiner's action (See MPEP 37 CFR 1.111(b)).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See attached PTO-892.

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) days from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).

When responding to the office action, Applicant is advised to clearly point out the

patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. ' 1.111(c).

When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Hong Kim whose telephone number is (703) 305-3835. The Examiner can normally be reached on the weekdays from 8:30 AM to 5:00 PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Matt Kim, can be reached on (703) 305-3821.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to TC-2100:
(703) 872-9306

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

HK
Primary Patent Examiner
May 2, 2004